digii MENTO

EDUCATING ON GO...

DIGITAL LOGIC

WorkBook

2018

DigiiMento Educational Service Pvt. Ltd.

Q1. (673.23)10 convert this decimal number into octal number system?

Note : Convert till 4 decimal positions. Ex: if your answer is 6565.414687.

Write answer as 6565.4146

Q2. Duality of the function F = X'YZ+XY'+YZ'

a. (X+Y'+Z').(X'+Y').(Y+Z')

b. (X'+Y+Z).(X+Y').(Y+Z')

c. (X'+Y+Z).(X+Y').(Y+Z)

d. None of these

Q3. If number of one's even then EX OR output?

Q4. The maximum no of self-dual functions with 3 Boolean variables is?

a. 32

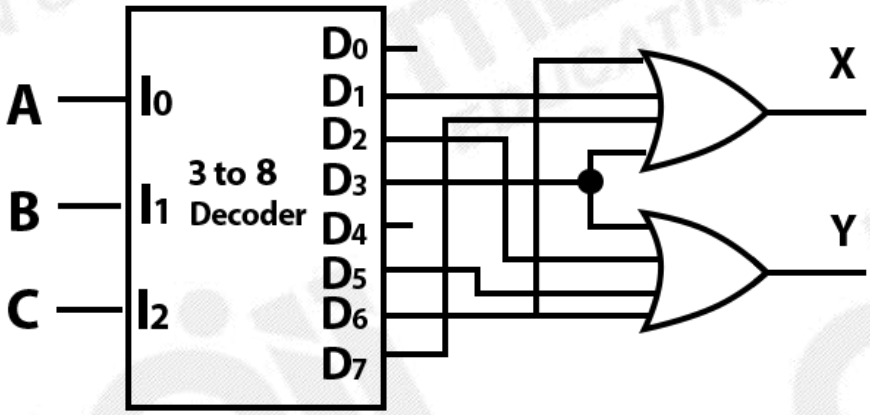
b. 256

c. 16

d. None of these

Q5.

The output of X is a. A'C+AB



a. A'C+AB

b. AC'+BC

c. AC+BC

d. AC'+ BC'

Q6.

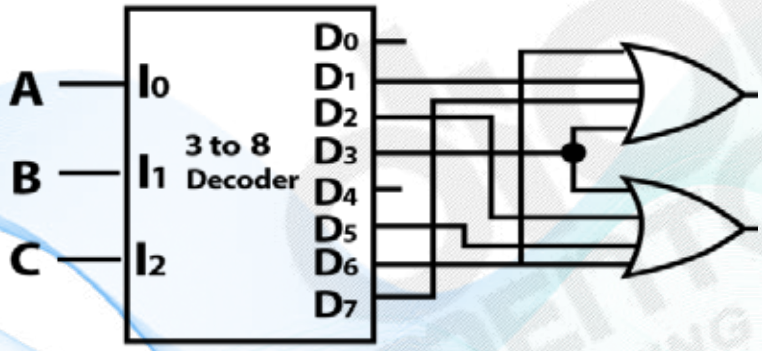
The output of Y is

a. A'B+BC'+A'B'C

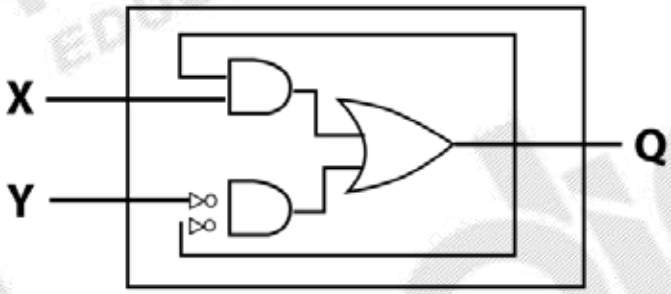
b. BC'+BA+AB'C

c. BC'+BA'+CB'A

d. None of these



Q7. Consider the given XY flip-flop



What values of X, Y respectively put flip flop in SET mode?

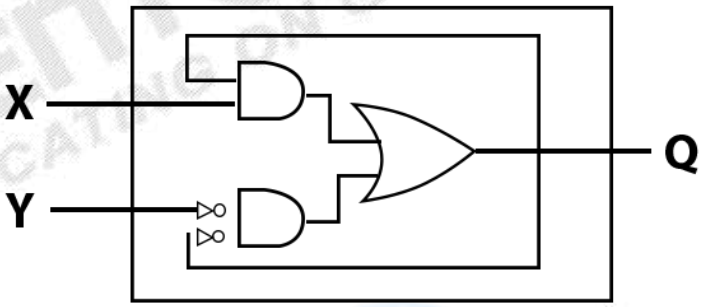
a. 0, 0

b. 0, 1

c. 1, 0

d. 1, 1

Q8. Consider the given XY flip-flop



What are the values of X, Y respectively to change the state of flip flop from 1 to 0?

a. 0, 0

b. 0, 1

c. 1, 0

d. 1, 1

Q9. Number of 2*1 MUXes used in level 3 to construct a 64*1 MUX are _____. Where the number of MUXes used gets reduced from level 1 to level N.

Q10. The minimum no of NOR gates required to implement the function F = AB+A'B

a. 4

b. 5

c. 2

d. 8

Q11. F (A, B, C, D) = Σm (1,2,3…..15). Simplified expression of the function F

a. 1

b. A+B+C

c. A+B+C+D'

d. A+B+C+D

Q12. Which gates do not follow the Associative law?

a. AND Gate

b. Universal Gate

c. Ex-OR Gate

d. None of these

Q13. Number of input conditions that will produce low output in an N input NOR Gate is?

a.2^N-1

b. 1

c. 2^N-N

d. N

Q14. A register contains 2' complement number 10100. When this register value is divided by 2 then the value at the o/p of register in decimal is?

Q15. Which of the given options is invalid

a. 256 x 1 MUX

b. 4 x 10 Decoder

c. 7 x 256 decode

d. 1 x 256 DEMUX

Q16. How many 2 I/P NAND gates required to recognize 2 I/P Ex-NOR gate?

a. 3

b. 4

c. 5

d. 6

Q17. How many 2 I/P NAND gates required to recognize full Sub-tractor?

Q18. Consider the following multiplication

(10w1z)2 x (15)10 =(y01011001)2

Which one of the following gives appropriate values of w, y and z.

a. w=0, y=0, z=1

b. w=0, y=1, z=1

c. w=1, y=1, z=0

d. w=1, y=1, z=1

Q19. Simplify the given Boolean expression using the Boolean algebra properties:

$v + v'w + v'w'x + v'w'x'y + v'w'x'y'z$

a. $v' + w + x + y + z$

b. $v + w + x + y + z$

c. $v' + w + x' + y + z$

d. $v' + w' + x + y + z$

Q20. Convert $(1220212120)_3$ into $(?)_9$?

a. 67765

b. 56775

c. 67756

d. 56776

Q21. The negative decimal number –N in the 2's complement representation is 1011. Then the representation for – (N+1) is?

a. 1100

b. 1110

c. 1010

d. 1101

Q22. The switching expression corresponding to f(A,B,C,D) = Σ(1, 4, 5, 9, 11, 12) is

a. BC'D'+A'C'D+AB'D

b. ABC'+ACD+B'C'D

c. ACD'+A'B'C'+AC'D'

d. A'BD+ACD'+BCD'

Q23. Consider the following Boolean function of 4 variables f(w, x, y, z)=Σ(1, 3, 4, 6, 9, 11, 12, 14). The function is

a. Independent of one variable

b. Independent of two variables

c. Independent of three variables

d. Dependent on all the variables

Q24. How many number of prime-implicants for the given function f(A, B, C, D)= Σm (0, 2, 5, 6, 7)

Q25. The minterm of f(P, Q, R) = PQ+QR'+PR' is

a. m2+m4+m6+m7

b. m0+m1+m6+m7

c. m0+m1+m3+m7

d. m2+m4+m5+m7

Q26. If x'y' =0, then x⊕y is

a. x+y

b. x' + y'

c. x+y'

d. x'+y

Q27.

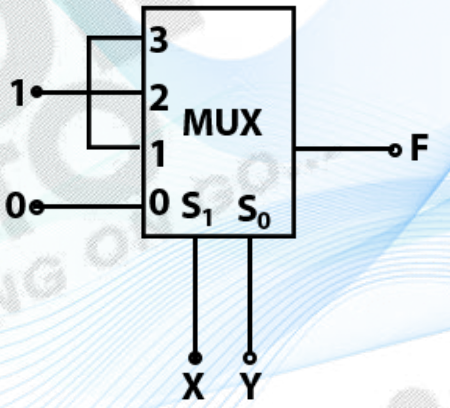
a. (xy)' +x

b. x + y

c. x'+ y'

d. 'xy+ x

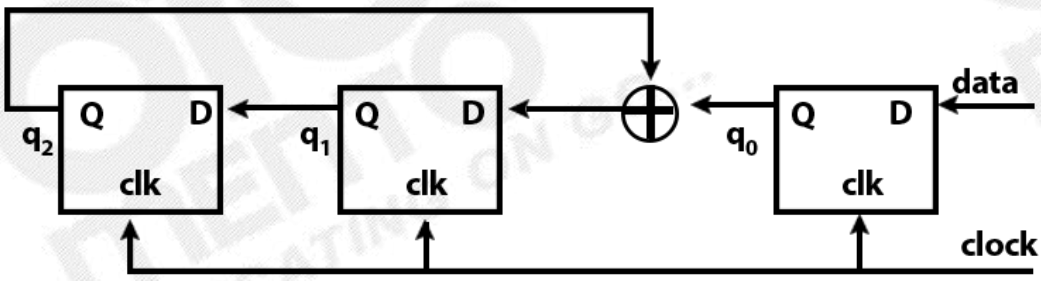
The Output F of the 4-to-1 MUX shown in figure is



Q28. Consider the equation $(43)_x = (y3)_8$ where 'x' and 'y' are unknown. The number of possible solutions is_____.

a. 3
b. 4
c. 5
d. 6

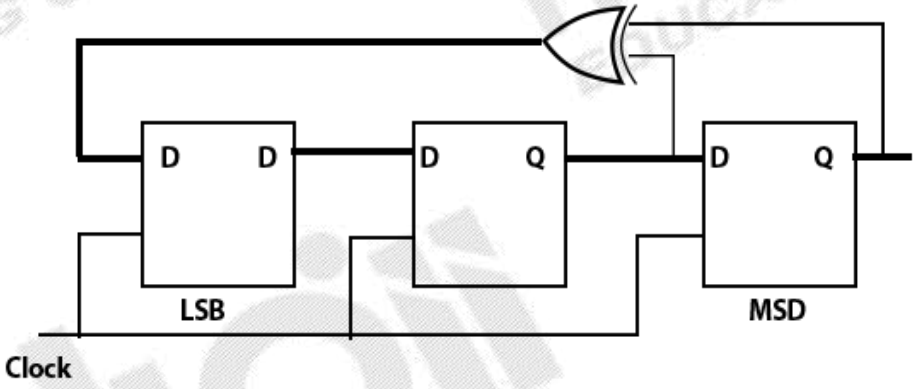
Q29. Consider the circuit in the diagram. The $\oplus$ operator represents Ex-OR. The D flipflops are initialized to zeroes (cleared).



The following data: 100110000 is supplied to the "data" terminal in nine clock cycles. After that the values of q2 q1 q0are:

a. 000
b. 001
c. 010
d. 101

Q30. Consider the circuit given below with initial state $Q_0 = 1$, $Q_1 = Q_2 = 0$. The state of the circuit is given by the value $4Q_2 + 2Q_1 + Q_0$. LSB output is denoted by Q_0, and MSB output is denoted by Q_2.



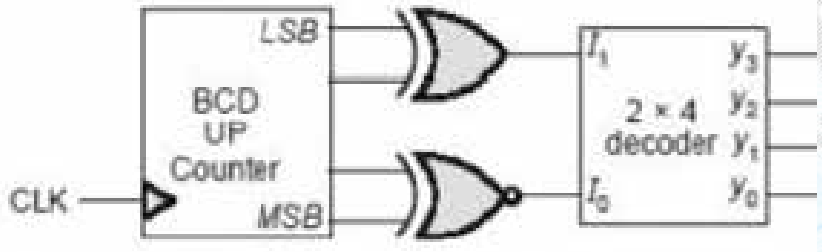
Which one of the following is the correct state sequence of the circuit?

a. 1,3,4,6,7,5,2
b. 1,2,5,3,7,6,4
c. 1,2,7,3,5,6,4
d. 1,6,5,7,2,3,4

Q31.

a. 2 clock pulses
b. 3 clock pulses
c. 10 clock pulses
d. 6 clock pulses

For the circuit shown below:



For how many number of clock pulses for which y_2 is '1'?

Q32.

a. 251

b. 253

c. 254

d. 255

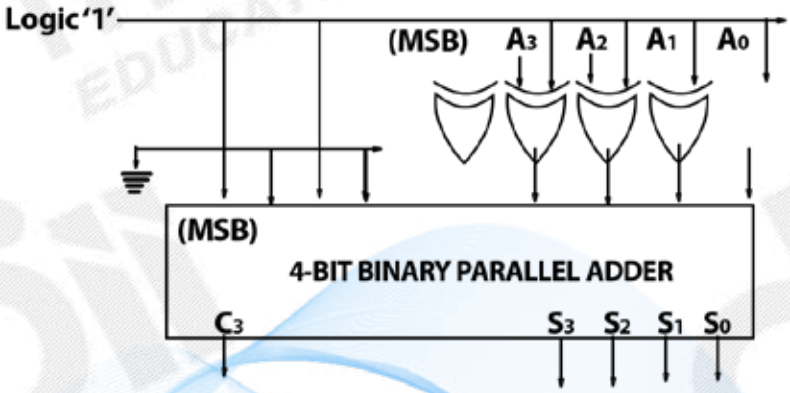
For the circuit goven below. If A+10101010 and B = 11111111

What is the decimal equivalent of the output ?

Q33. Consider the digital circuit shown below

a. 9's complement circuit

b. 0's complement circuit

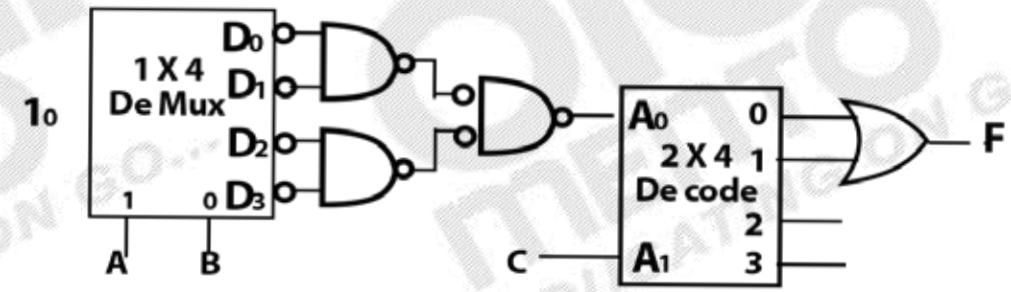


The digital circuit acts as

c. 5's complement circuit

d. 9's complement circuit if C3 = 0 and 10's complement circuit if C3 = 1.

Consider the logic circuit given below:



The minimized expression for F is

Q34.

a. C'

b. $/_0$

c. C

d. $/_0^1$

Q35. The Q-output of J-K flip-flop is 1. The output does not change when a clock pulse is applied. The input J and K will be respectively (x- don't care state)

a. 0 and x

b. 0 and 1

c. 1 and 0

d. x and 0

Q36. In a right shift register, right shift operation of binary 11 gives

a. 5.5

b. 5

c. 6

d. None of these

Q37.

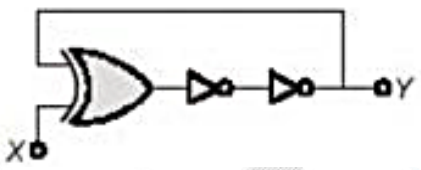
a. X = 0

b. X = 1

c. X = 0 or 1

d. X = Y

All the logic gates in the circuit shown below have finite propagation delay. The circuit can be used as a clock generator, if



Q38. X-Y flip flop, whose characteristics Table is given below is to be implement using a J-K flip flop

This can be done by making

a. J= Y', K=X

b. J=Y, K=X'

c. J=X, K=Y'

d. J=X', K=Y

X	Y	Q_{n+1}
0	0	1
0	1	Q'_{n+1}
1	0	Q_n
1	1	0

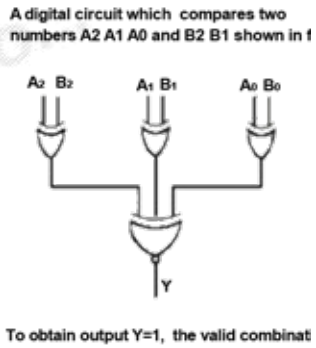
Q39.

a. 010, 111

b. 101, 110

c. 010, 101

d. 101, 011



Q40.

a. Π M(4, 6)

b. Σ m(0, 1, 2, 3, 5, 7)

c. Σ m(4, 6)

d. Π M(0, 1, 2, 3, 5)