101. The memory blocks are mapped on to the cache with the help of _____

a) Hash functions
b) Vectors
c) Mapping functions
d) None of the mentioned

102. During a write operation if the required block is not present in the cache then _____ occurs.

a) Write latency
b) Write hit
c) Write delay
d) Write miss

103. In _____ protocol the information is directly written into main memory.

a) Write through
b) Write back
c) Write first
d) None of the mentioned

104. The only drawback of using the early start protocol is _____

a) Time delay
b) Complexity of circuit
c) Latency
d) High miss rate

105. The method of mapping the consecutive memory blocks to consecutive cache blocks is called _____

a) Set associative
b) Associative
c) Direct
d) Indirect

106. While using the direct mapping technique, in a 16-bit system the higher order 5 bits is used for _____

a) Tag
b) Block
c) Word
d) Id

107. In direct mapping the presence of the block in memory is checked with the help of block field.

a) True

b) False

108. In associative mapping, in a 16-bit system the tag field has _____ bits.

a) 12

b) 8

c) 9

d) 10

109. The associative mapping is costlier than direct mapping.

a) True

b) False

110. The technique of searching for a block by going through all the tags is _____

a) Linear search

b) Binary search

c) Associative search

d) None of the mentioned

111. The set associative map technique is a combination of the direct and associative technique.

a) True

b) False

112. In set-associative technique, the blocks are grouped into _____ sets.

a) 4

b) 8

c) 12

d) 6

113. A control bit called ____ has to be provided to each block in set-associative.

a) Idol bit
b) Valid bit
c) Reference bit
d) All of the mentioned

114. The bit used to indicate whether the block was recently used or not is _____

a) Idol bit
b) Control bit
c) Reference bit
d) Dirty bit

115. Data which is not up-to date is called as _____

a) Spoilt data
b) Stale data
c) Dirty data
d) None of the mentioned

116. The main memory is structured into modules each with its own address register called _____

a) ABR
b) TLB
c) PC
d) IR

117. When consecutive memory locations are accessed only one module is accessed at a time.

a) True

b) False

118. In memory interleaving, the lower order bits of the address are used to

a) Get the data

b) Get the address of the module

c) Get the address of the data within the module

d) None of the mentioned

119. The number successful accesses to memory stated as a fraction is called as _____

a) Hit rate
b) Miss rate
c) Success rate
d) Access rate

120. The number failed attempts to access memory, stated in the form of fraction is called as _____

a) Hit rate
b) Miss rate
c) Failure rate
d) Delay rate

121. In associative mapping during LRU, the counter of the new block is set to ‘0’ and all the others are incremented by one, when _____ occurs.

a) Delay
b) Miss
c) Hit
d) Delayed hit

122. If hit rates are well below 0.9, then they’re called as speedy computers.
a) True
b) False

123. The extra time needed to bring the data into memory in case of a miss is called as _____
a) Delay
b) Propagation time
c) Miss penalty
d) None of the mentioned

124. _____ are the different type/s of generating control signals.

a) Micro-programmed
b) Hardwired
c) Micro-instruction
d) Both Micro-programmed and Hardwired

125. The type of control signal are generated based on,

a) contents of the step counter
b) Contents of IR
c) Contents of condition flags
d) All of the mentioned

126. What does the end instruction do?
a) It ends the generation of a signal
b) It ends the complete generation process
c) It starts a new instruction fetch cycle and resets the counter
d) It is used to shift the control to the processor

127. The name hardwired came because the sequence of operations carried out are determined by the wiring.
a) True
b) False

128. The benefit of using this approach is

a) It is cost effective

b) It is highly efficient

c) It is very reliable

d) It increases the speed of operation

129. The disadvantage/s of the hardwired approach is

a) It is less flexible

b) It cannot be used for complex instructions

c) It is costly

d) less flexible & cannot be used for complex instructions

130. In micro-programmed approach, the signals are generated by _____

a) Machine instructions
b) System programs
c) Utility tools
d) None of the mentioned

131. A word whose individual bits represent a control signal is _____

a) Command word
b) Control word
c) Co-ordination word
d) Generation word

132. A sequence of control words corresponding to a control sequence is called _____

a) Micro routine
b) Micro function
c) Micro procedure
d) None of the mentioned

133. Individual control words of the micro routine are called as _____

a) Micro task
b) Micro operation
c) Micro instruction
d) Micro command

134. The special memory used to store the micro routines of a computer is _____

a) Control table
b) Control store
c) Control mart
d) Control shop

135. To read the control words sequentially _____ is used.

a) PC
b) IR
c) UPC
d) None of the mentioned

136. Every time a new instruction is loaded into IR the output of _____ is loaded into UPC.
a) Starting address generator
b) Loader
c) Linker
d) Clock

137. The signals are grouped such that mutually exclusive signals are put together.
a) True
b) False

138. Highly encoded schemes that use compact codes to specify a small number of functions in each micro instruction is _____

a) Horizontal organisation
b) Vertical organisation
c) Diagonal organisation
d) None of the mentioned

139. The directly mapped cache no replacement algorithm is required.

a) True
b) False

140. The algorithm which replaces the block which has not been referenced for a while is called _____

a) LRU
b) ORF
c) Direct
d) Both LRU and ORF

141. The counter that keeps track of how many times a block is most likely used is _____

a) Count
b) Reference counter
c) Use counter
d) Probable counter

142. _____ have been developed specifically for pipelined systems.

a) Utility software
b) Speed up utilities
c) Optimizing compilers
d) None of the mentioned

143. Each stage in pipelining should be completed within ____ cycle.

a) 1
b) 2
c) 3
d) 4

144. To increase the speed of memory access in pipelining, we make use of _____

a) Special memory locations
b) Special purpose registers
c) Cache
d) Buffers

145. The periods of time when the unit is idle is called as _____

a) Stalls
b) Bubbles
c) Hazards
d) Both Stalls and Bubbles

146. The contention for the usage of a hardware device is called as _____

a) Structural hazard
b) Stalk
c) Deadlock
d) None of the mentioned

147. The situation where in the data of operands are not available is called _____

a) Data hazard
b) Stock
c) Deadlock
d) Structural hazard

148. The computer architecture aimed at reducing the time of execution of instructions is _____

a) CISC
b) RISC
c) ISA
d) ANNA

149. The RISC processor has a more complicated design than CISC.

a) True
b) False

150. The iconic feature of the RISC machine among the following are

a) Reduced number of addressing modes

b) Increased memory size

c) Having a branch delay slot

d) All of the mentioned