51. The type of memory assignment used in Intel processors is _____

a) Little Endian
b) Big Endian
c) Medium Endian
d) None of the mentioned

52. When using the Big-Endian assignment to store a number, the sign bit of the number is stored in _____

a) The higher order byte of the word
b) The lower order byte of the word
c) Can’t say
d) None of the mentioned

53. To get the physical address from the logical address generated by CPU we use ____

a) MAR
b) MMU
c) Overlays
d) TLB

54. During transfer of data between the processor and memory we use _____

a) Cache
b) TLB
C) Buffers
d) Registers

55. Physical memory is divided into sets of finite size called as _____

a) Frames
b) Pages
c) Blocks
d) Vectors

56. In a system, which has 32 registers the register id is ____ long.

a) 16 bit
b) 8 bits
c) 5 bits
d) 6 bits

57. The two phases of executing an instruction are _____

a) Instruction decoding and storage
b) Instruction fetch and instruction execution
c) Instruction execution and storage
d) Instruction fetch and Instruction processing

58. The Instruction fetch phase ends with _____

a) Placing the data from the address in MAR into MDR
b) Placing the address of the data into MAR
c) Completing the execution of the data and placing its storage address into MAR
d) Decoding the data in MDR and placing it in IR

59. When using Branching, the usual sequencing of the PC is altered. A new instruction is loaded which is called as _____

a) Branch target
b) Loop target
c) Forward target
d) Jump instruction

60. The condition flag Z is set to 1 to indicate _____

a) The operation has resulted in an error
b) The operation requires an interrupt call
c) The result is zero
d) There is no empty register available

61. ____ converts the programs written in assembly language into machine instructions.

a) Machine compiler
b) Interpreter
c) Assembler
d) Converter

62. The instructions like MOV or ADD are called as _____

a) OP-Code
b) Operators
c) Commands
d) None of the mentioned

63. The alternate way of writing the instruction, ADD #5, R1 is _____

a) ADD [5], [R1];
b) ADDI 5, R1;
c) ADDIME 5, [R1];
d) There is no other way

64. The last statement of the source program should be _____

a) Stop
b) Return
c) OP
d) End

65. The assembler stores all the names and their corresponding values in _____

a) Special purpose Register
b) Symbol Table
c) Value map Set
d) None of the mentioned

66. The return address of the Sub-routine is pointed to by _____

a) IR
b) PC
c) MAR
d) Special memory registers

67. The location to return to, from the subroutine is stored in _____

a) TLB
b) PC
c) MAR
d) Link registers

68. The advantage of I/O mapped devices to memory mapped is

a) The former offers faster transfer of data
b) The devices connected using I/O mapping have a bigger buffer space
c) The devices have to deal with fewer address lines
d) No advantage as such

69. The system is notified of a read or write operation by

a) Appending an extra bit of the address
b) Enabling the read or write bits of the devices
c) Raising an appropriate interrupt signal
d) Sending a special signal along the BUS

70. To overcome the lag in the operating speeds of the I/O device and the processor we use

a) Buffer spaces
b) Status flags
c) Interrupt signals
d) Exceptions

71. The method of accessing the I/O devices by repeatedly checking the status flags is

a) Program-controlled I/O
b) Memory-mapped I/O
c) I/O mapped
d) None of the mentioned

72. The method which offers higher speeds of I/O transfers is

a) Interrupts
b) Memory mapping
c) Program-controlled I/O
d) DMA

73. The process where in the processor constantly checks the status flags is called as

a) Polling
b) Inspection
c) Reviewing
d) Echoing

74. The interrupt-request line is a part of the

a) Data line
b) Control line
c) Address line
d) None of the mentioned

75. The signal sent to the device from the processor after receiving an interrupt is

a) Interrupt-acknowledge
b) Return signal
c) Service signal
d) Permission signal

76. Interrupts form an important part of _____ systems.

a) Batch processing
b) Multitasking
c) Real-time processing
d) Multi-user

77. A single Interrupt line can be used to service n different devices?

a) True

b) False

78. CPU as two modes privileged and non-privileged. In order to change the mode from privileged to non-privileged

a) A hardware interrupt is needed

b) A software interrupt is needed

c) Either hardware or software interrupt is needed

d) A non-privileged instruction (which does not generate an interrupt) is needed

79. Which interrupt is unmaskable?

a) RST 5.5
b) RST 7.5
c) TRAP
d) Both RST 5.5 and 7.5

80. How can the processor ignore other interrupts when it is servicing one

a) By turning off the interrupt request line
b) By disabling the devices from sending the interrupts
c) BY using edge-triggered request lines
d) All of the mentioned

81. The DMA differs from the interrupt mode by

a) The involvement of the processor for the operation
b) The method accessing the I/O devices
c) The amount of data transfer possible
d) None of the mentioned

82. The DMA transfers are performed by a control circuit called as

a) Device interface
b) DMA controller
c) Data controller
d) Overlooker

83. In DMA transfers, the required signals and addresses are given by the

a) Processor
b) Device drivers
c) DMA controllers
d) The program itself

84. After the completion of the DMA transfer the processor is notified by

a) Acknowledge signal
b) Interrupt signal
c) WMFC signal
d) None of the mentioned

85. The controller is connected to the ____

a) Processor BUS
b) System BUS
c) External BUS
d) None of the mentioned

86. The technique whereby the DMA controller steals the access cycles of the processor to operate is called

a) Fast conning
b) Memory Con
c) Cycle stealing
d) Memory stealing

87. The technique where the controller is given complete access to main memory is

a) Cycle stealing
b) Memory stealing
c) Memory Con
d) Burst mode

88. When process requests for a DMA transfer

a) Then the process is temporarily suspended
b) The process continues execution
c) Another process gets executed
d) process is temporarily suspended & Another process gets executed

89. The DMA transfer is initiated by _____

a) Processor

b) The process being executed

c) I/O devices

d) OS

90. The standard SRAM chips are costly as _____

a) They use highly advanced micro-electronic devices

b) They house 6 transistors per chip

c) They require specially designed PCB's

d) None of the mentioned

91. The drawback of building a large memory with DRAM is _____

a) The large cost factor
b) The inefficient memory organisation
c) The Slow speed of operation
d) All of the mentioned

92. The fastest data access is provided using _____

a) Caches
b) DRAM’s
c) SRAM’s
d) Registers

93. The memory which is used to store the copy of data or instructions stored in larger memories, inside the CPU is called _____

a) Level 1 cache
b) Level 2 cache
c) Registers
d) TLB

94. The larger memory placed between the primary cache and the memory is called _____

a) Level 1 cache
b) Level 2 cache
c) EEPROM
d) TLB

95. The last on the hierarchy scale of memory devices is _____

a) Main memory

b) Secondary memory

c) TLB

d) Flash drives

96. In the memory hierarchy, as the speed of operation increases the memory size also increases.

a) True

b) False

97. The reason for the implementation of the cache memory is _____

a) To increase the internal memory of the system
b) The difference in speeds of operation of the processor and memory
c) To reduce the memory access and cycle time
d) All of the mentioned

98. The effectiveness of the cache memory is based on the property of _____

a) Locality of reference
b) Memory localisation
c) Memory size
d) None of the mentioned

99. The temporal aspect of the locality of reference means

a) That the recently executed instruction won't be executed soon
b) That the recently executed instruction is temporarily not referenced
c) That the recently executed instruction will be executed soon again
d) None of the mentioned

100. The spatial aspect of the locality of reference means

a) That the recently executed instruction is executed again next

b) That the recently executed won't be executed again

c) That the instruction executed will be executed at a later time

d) That the instruction in close proximity of the instruction executed will be executed in future