1. The ___ format is usually used to store data.
a) $B C D$
b) Decimal
c) Hexadecimal
d) Octal
2. A source program is usually in
a) Assembly language
b) Machine level language
c) High-level language
d) Natural language
3. Which memory device is generally made of semiconductors?
a) RAM
b) Hard-disk
c) Floppy disk
d) Cd disk
4. The small extremely fast, RAM's are called as
a) Cache
b) Heaps
c) Accumulators
d) Stacks
5. The ALU makes use of $\qquad$ to store the intermediate results.
a) Accumulators
b) Registers
c) Heap
d) Stack
6. The control unit controls other units by generating
a) Control signals
b) Timing signals
c) Transfer signals
d) Command Signals
7. ___ are numbers and encoded characters, generally used as operands.
a) Input
b) Data
c) Information
d) Stored Values
9.__bus structure is usually used to connect I/O
devices.
a) Single bus
b) Multiple bus
c) Star bus
d) Rambus
8. The I/O interface required to connect the I/O device to the bus consists of $\qquad$
a) Address decoder and registers
b) Control circuits
c) Address decoder, registers and Control circuits
d) Only Control circuits
9. To reduce the memory access time we generally make use of $\qquad$
a) Heaps
b) Higher capacity RAM’s
c) SDRAM's
d) Cache's
10. ___ is generally used to increase the apparent size of physical memory.
a) Secondary memory
b) Virtual memory
c) Hard-disk
d) Disks
11. The time delay between two successive initiation of memory operation
a) Memory access time
b) Memory search time
c) Memory cycle time
d) Instruction delay
12. The decoded instruction is stored in $\qquad$
a) IR
b) PC
c) Registers
d) MDR
13. The instruction -> Add LOCA, R0 does $\qquad$
a) Adds the value of LOCA to R0 and stores in the temp register
b) Adds the value of R0 to the address of LOCA
c) Adds the values of both LOCA and R0 and stores it in R0
d) Adds the value of LOCA with a value in accumulator and stores it in R0
14. Which registers can interact with the secondary storage?
a) MAR
b) PC
c) IR
d) R0
15. During the execution of a program which gets initialized first?
a) MDR
b) IR
c) PC
d) MAR
16. Which of the register/s of the processor is/are connected to Memory Bus?
a) PC
b) MAR
c) IR
d) Both PC and MAR
17. The internal Components of the processor are connected by
a) Processor intra-connectivity circuitry
b) Processor bus
c) Memory bus
d) Rambus
18. The registers, ALU and the interconnection between them are collectively called as $\qquad$
a) process route
b) information trail
c) information path
d) data path
19. ANSI stands for
a) American National Standards Institute
b) American National Standard Interface
c) American Network Standard Interfacing
d) American Network Security Interrupt
20. The main advantage of multiple bus organisation over single bus is $\qquad$
a) Reduction in the number of cycles for execution
b) Increase in size of the registers
c) Better Connectivity
d) None of the mentioned
21. During the execution of the instructions, a copy of the instructions is placed in the
a) Register
b) RAM
c) System heap
d) Cache
22. A processor performing fetch or decoding of different instruction during the execution of another instruction is called $\qquad$
a) Super-scaling
b) Pipe-lining
c) Parallel Computation
d) None of the mentioned
23. An optimizing Compiler does
a) Better compilation of the given piece of code
b) Takes advantage of the type of processor and reduces its process time
c) Does better memory management
d) none of the mentioned
24. The ultimate goal of a compiler is to
a) Reduce the clock cycles for a programming task
b) Reduce the size of the object code
c) Be versatile
d) Be able to detect even the smallest of errors
25. When Performing a looping operation, the instruction gets stored in the
a) Registers
b) Cache
c) System Heap
d) System stack
26. The average number of steps taken to execute the set of instructions can be made to be less than one by following
a) ISA
b) Pipe-lining
c) Super-scaling
d) Sequential

## 31. CISC stands for

a) Complete Instruction Sequential Compilation
b) Computer Integrated Sequential Compiler
c) Complex Instruction Set Computer
d) Complex Instruction Sequential Compilation
32. The instruction, ADD \#45, R1 does $\qquad$
a) Adds the value of 45 to the address of R1 and stores 45 in that address
b) Adds 45 to the value of R1 and stores it in R1
c) Finds the memory location 45 and adds that content to that of R1
d) None of the mentioned
33. In case of, Zero-address instruction method the operands are stored in $\qquad$
a) Registers
b) Accumulators
c) Push down stack
d) Cache
34. Add \#45, when this instruction is executed the following happen/s $\qquad$
a) The processor raises an error and requests for one more operand
b) The value stored in memory location 45 is retrieved and one more operand is requested
c) The value 45 gets added to the value on the stack and is pushed onto the stack
d) None of the mentioned
35. The addressing mode which makes use of in-direction pointers is $\qquad$
a) Indirect addressing mode
b) Index addressing mode
c) Relative addressing mode
d) Offset addressing mode
36. In the following indexed addressing mode instruction, MOV 5(R1), LOC the effective address is $\qquad$
a) $E A=5+R 1$
b) $E A=R 1$
c) $E A=[R 1]$
d) $E A=5+[R 1]$
37. The addressing mode/s, which uses the PC instead of a general-purpose register is $\qquad$
a) Indexed with offset
b) Relative
c) direct
d) both Indexed with offset and direct
38. The addressing mode, where you directly specify the operand value is $\qquad$
a) Immediate
b) Direct
c) Definite
d) Relative
39. The effective address of the following instruction is, MUL 5(R1, R2).
a) $5+R 1+R 2$
b) $5+(\mathrm{R} 1 * \mathrm{R} 2)$
c) $5+[\mathrm{R} 1]+[\mathrm{R} 2]$.
d) $5^{*}([\mathrm{R} 1]+[\mathrm{R} 2])$
40. ___ addressing mode is most suitable to change the normal sequence of execution of instructions.
a) Relative
b) Indirect
c) Index with Offset
d) Immediate
41. Which method/s of representation of numbers occupies large amount of memory than others?
a) Sign-magnitude
b) 1's compliment
c) 2's compliment
d) 1's \& 2's compliment
42. Which representation is most efficient to perform arithmetic operations on the numbers?
a) Sign-magnitude
b) 1's compliment
c) 2'S compliment
d) None of the mentioned
43. Which method of representation has two representations for ' 0 '?
a) Sign-magnitude
b) 1's compliment
c) 2's compliment
d) None of the mentioned
44. When we perform subtraction on -7 and 1 the answer in 2's compliment form is
a) 1010
b) 1110
c) 0110
d) 1000
45. When we perform subtraction on -7 and -5 the answer in 2's compliment form is $\qquad$
a) 11110
b) 1110
c) 1010
d) 0010
46. The processor keeps track of the results of its operations using a flag called
a) Conditional code flags
b) Test output flags
c) Type flags
d) None of the mentioned
47. The register used to store the flags is called as
a) Flag register
b) Status register
c) Test register
d) Log register

## 48. The Flag ' $V$ ' is set to 1 indicates that,

a) The operation is valid
b) The operation is validated
c) The operation as resulted in an overflow
d) None of the mentioned
49. The most efficient method followed by computers to multiply two unsigned numbers is
a) Booth algorithm
b) Bit pair recording of multipliers
c) Restoring algorithm
d) Non-restoring algorithm
50. When 1101 is used to divide 100010010 the remainder is
a) 101
b) 11
c) 0
d) 1

